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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,467	10/07/2003	Terunao Hanaoka	117462	6659

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EXAMINER	
TRAN, THANH Y	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,467	TERUNAO HANAOKA	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18 and 23-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-17 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al (U.S. 6,891,248) in view of Hashimoto (U.S. 6,323,542) and Irie (U.S. 6,534,386).

As to claim 11, Akram et al discloses in figure 1E a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming a redistribution layer (comprising "power conductor" 42Vcc and "electrode" 36) over a semiconductor wafer ("die" 12) which includes an integrated circuit (24) and an interconnect (comprising "conductor" 22 and "power die contact" 16Vcc) electrically connected with the integrated circuit (24), the redistribution layer (comprising "power conductor" 42Vcc and "electrode" 36) electrically connecting with a pad ("power die contact" 16Vcc) which is a part of the interconnect (comprising "conductor" 22 and "power die contact" 16Vcc) and including a first portion located over the pad ("power die contact" 16Vcc) and a second section other than the first portion; forming an external terminal ("power terminal contact" 14Vcc) on the second section of the redistribution layer (comprising "power conductor" 42Vcc and "electrode" 36).

Akram et al does not disclose a semiconductor device comprising: forming a first resin layer having a side surface so that at least a part of the first resin layer is placed on the

redistribution layer; forming a second resin layer over the first resin layer and on the semiconductor wafer so as to cover the side surface of the first resin layer.

Hashimoto discloses in figure 8 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming a first resin layer ("stress relieving layer"57) [*"stress relieving layer" can be silicon denatured polyimide resin or epoxy resin or silicone denatured epoxy resin*, see col. 7, lines 13-19] having a side surface [*a side surface is the extended outer surface (curved surface) of layer 57*] so that at least a part of the first resin layer (57) is placed on the redistribution layer ("wiring" 58); forming a second resin layer ("supplementary transmission layer" 53) [*"supplementary transmission layer" is constructed of resin*, see col. 9, lines 25-36] over the first resin layer (57) and on the semiconductor wafer (52) so as to cover the side surface of the first resin layer (57). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Akram et al by forming a first resin layer having a side surface so that at least a part of the first resin layer is placed on the redistribution layer; and forming a second resin layer over the first resin layer and on the semiconductor wafer so as to cover the side surface of the first resin layer as taught by Hashimoto for protecting the redistribution layer (wiring) and the semiconductor chip of the semiconductor device (see col. 11, lines 56-58 in Hashimoto).

Akram et al in view of Hashimoto does not disclose the step of cutting the semiconductor wafer. Irie (U.S. 6,534,386) discloses in figures 2-3 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: cutting the semiconductor wafer (101) (see col. 1, lines 25-39). Therefore, it would have been obvious to a person having

ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of Akram et al in view of Hashimoto by having the step of cutting the semiconductor wafer as taught by Irie for providing individual semiconductor chips for use in the other devices (see col. 1, lines 25-39 in Irie).

As to claim 12, Akram et al does not a semiconductor device comprising: forming the first resin layer to cover the redistribution layer excluding a region in which the external terminal is formed, and forming the second resin layer to cover at least a lower part of the external terminal.

Hashimoto discloses in figure 8 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming a first resin layer ("stress relieving layer"57) ["*stress relieving layer" can be silicon denatured polyimide resin or epoxy resin or silicone denatured epoxy resin*, see col. 7, lines 13-19] to cover the redistribution layer ("wiring" 58) excluding a region in which the external terminal ("solder ball" 60) is formed, and forming the second resin layer ("supplementary transmission layer" 53) ["*supplementary transmission layer" is constructed of resin*, see col. 9, lines 25-36] to cover at least a lower part of the external terminal ("solder ball" 60). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Akram et al by forming the first resin layer to cover the redistribution layer excluding a region in which the external terminal is formed, and forming the second resin layer to cover at least a lower part of the external terminal as taught by Hashimoto for protecting the redistribution layer (wiring) and the semiconductor chip of the semiconductor device (see col. 11, lines 56-58 in Hashimoto); also for retaining the external terminal within the semiconductor device.

As to claim 13, Akram et al discloses in figure 1E a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming an insulating layer ("dielectric layer" 38) before forming the redistribution layer (comprising "power conductor" 42Vcc and "electrode" 36), wherein the redistribution layer (comprising "power conductor" 42Vcc and "electrode" 36) is formed on the insulating layer ("wiring" 38).

As to claims 14, 15 and 16, figure 6A of Akram et al shows the semiconductor wafer (10W) includes a first region [*a first region is a spaced region between the regions of dices 12W*] and a plurality of second regions [*a plurality of second regions are the regions of dices 12W*], each of the second regions being surrounded by the first region.

Akram et al does not disclose the first resin layer and the second resin layer are formed only in the second region.

Hashimoto discloses in figure 8 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming a first resin layer ("stress relieving layer"57) ["*stress relieving layer" can be silicon denatured polyimide resin or epoxy resin or silicone denatured epoxy resin*, see col. 7, lines 13-19] and the second resin layer ("supplementary transmission layer" 53) ["*supplementary transmission layer" is constructed of resin*, see col. 9, lines 25-36]) are formed only in the second region [the second region is the region of the semiconductor wafer (die/chip 52)]. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Akram et al by forming the first resin layer and the second resin layer only in the second region as taught by Hashimoto for protecting the redistribution layer (wiring) and the semiconductor chip of the semiconductor device (see col. 11, lines 56-58 in Hashimoto).

Akram et al in view of Hashimoto does not disclose the semiconductor device comprising: the semiconductor wafer is cut along the first region. Irie (U.S. 6,534,386) discloses in figures 2-3 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: the semiconductor wafer (101) is cut along the first region ("dicing line" 102) (see col. 1, lines 25-39). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of Akram et al in view of Hashimoto by having the semiconductor wafer which is cut along the first region as taught by Irie for providing individual semiconductor chips for use in the other devices (see col. 1, lines 25-39 in Irie).

As to claim 17, Akram et al does not disclose a semiconductor device comprising: forming a part of the second resin layer which covers the side surface of the first resin layer, in a upper part and along an edge portion of the second region.

Hashimoto discloses in figure 8 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming a part of the second resin layer ("supplementary transmission layer" 53) ["*supplementary transmission layer" is constructed of resin*, see col. 9, lines 25-36] which covers the side surface of the first resin layer ("stress relieving layer"57) ["*stress relieving layer" can be silicon denatured polyimide resin or epoxy resin or silicone denatured epoxy resin*, see col. 7, lines 13-19], in a upper part and along an edge portion of the second region [the second region is the region of the semiconductor wafer (die/chip 52)]. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Akram et al by forming a part of the second resin layer which covers the side surface of the first resin layer, in

an upper part and along an edge portion of the second region as taught by Hashimoto for protecting the redistribution layer (wiring) and the semiconductor chip of the semiconductor device (see col. 11, lines 56-58 in Hashimoto).

As to claim 23, Akram et al discloses in figure 1E a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming a wiring pattern ("comprising "power conductor" 42Vcc and "electrode" 36") over a semiconductor wafer ("die" 12) which includes an integrated circuit (24) and an interconnect (comprising "conductor" 22 and "power die contact" 16Vcc) electrically connected with the integrated circuit (24), the wiring pattern (comprising "power conductor" 42Vcc and "electrode" 36) electrically connecting with a pad ("power die contact" 16Vcc) which is a part of the interconnect (comprising "conductor" 22 and "power die contact" 16Vcc) and including a first portion located over the pad ("power die contact" 16Vcc) and a second section other than the first portion; forming an external terminal ("power terminal contact" 14Vcc) on the second section of the wiring pattern (comprising "power conductor" 42Vcc and "electrode" 36).

Akram et al does not disclose a semiconductor device comprising: forming a first resin layer having a side surface so that at least a part of the first resin layer is placed on the wiring pattern; forming a second resin layer over the first resin layer and on the semiconductor wafer so as to cover the side surface of the first resin layer.

Hashimoto discloses in figure 8 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: forming a first resin layer ("stress relieving layer"57) [*"stress relieving layer" can be silicon denatured polyimide resin or epoxy resin or silicone denatured epoxy resin*, see col. 7, lines 13-19] having a side surface [*a side surface is the*

extended outer surface (curved surface) of layer 57] so that at least a part of the first resin layer (57) is placed on the wiring pattern ("wiring" 58); forming a second resin layer ("supplementary transmission layer" 53) ["*supplementary transmission layer" is constructed of resin*, see col. 9, lines 25-36] over the first resin layer (57) and on the semiconductor wafer (52) so as to cover the side surface of the first resin layer (57). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Akram et al by forming a first resin layer having a side surface so that at least a part of the first resin layer is placed on the wiring pattern; and forming a second resin layer over the first resin layer and on the semiconductor wafer so as to cover the side surface of the first resin layer as taught by Hashimoto for protecting the wiring pattern and the semiconductor chip of the semiconductor device (see col. 11, lines 56-58 in Hashimoto).

Akram et al in view of Hashimoto does not disclose the step of cutting the semiconductor wafer. Irie (U.S. 6,534,386) discloses in figures 2-3 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: cutting the semiconductor wafer (101) (see col. 1, lines 25-39). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of Akram et al in view of Hashimoto by having the step of cutting the semiconductor wafer as taught by Irie for providing individual semiconductor chips for use in the other devices (see col. 1, lines 25-39 in Irie).

As to claims 24 and 25, Akram et al does not disclose the second resin layer extending further along a surface of the semiconductor wafer than the first resin layer so as to cover a surface area of the semiconductor wafer that is not covered by the first resin layer.

Hashimoto further discloses in figure 9 a semiconductor device and a corresponding method of manufacturing a semiconductor device comprising: a second resin layer (77) extending further along a surface of the semiconductor wafer (72) than the first resin layer (76) so as to cover a surface area of the semiconductor wafer (72) that is not covered by the first resin layer (76). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of Akram et al by having a second resin layer extending further along a surface of the semiconductor wafer than the first resin layer so as to cover a surface area of the semiconductor wafer that is not covered by the first resin layer as taught by Hashimoto for absorbing the stress from the chip and the surface of the substrate.

3. Claim18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al (U.S. 6,891,248) in view of Hashimoto (U.S. 6,323,542) and Irie (U.S. 6,534,386) as applied to claim 11 above, and further in view of Teng (U.S. 6,242,156).

As to claim 18, Akram et al in view of Hashimoto and Irie does not disclose a semiconductor device comprising: the second resin layer is formed by using a resin that is sensitive to radiation and by applying lithographic technology.

Teng (U.S. 6,242,156) discloses in col. 8, line 61 – col. 9, line 11 a resin layer ("radiation-sensitive layer") is formed by using a resin ("diazo resin") that is sensitive to radiation and by applying lithographic technology. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Akram et al in view of Hashimoto and Irie by having a resin layer that

is formed by using a resin that is sensitive to radiation and by applying lithographic technology as taught by Teng in order to avoid the interference effects of radiation.

Response to Arguments

4. Applicant's arguments with respect to claims 11 and 23-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

ZANDRA V. SMITH
PRIMARY EXAMINER
27 Dec. 2005